# **CSE 620: Advanced Computer Architecture**

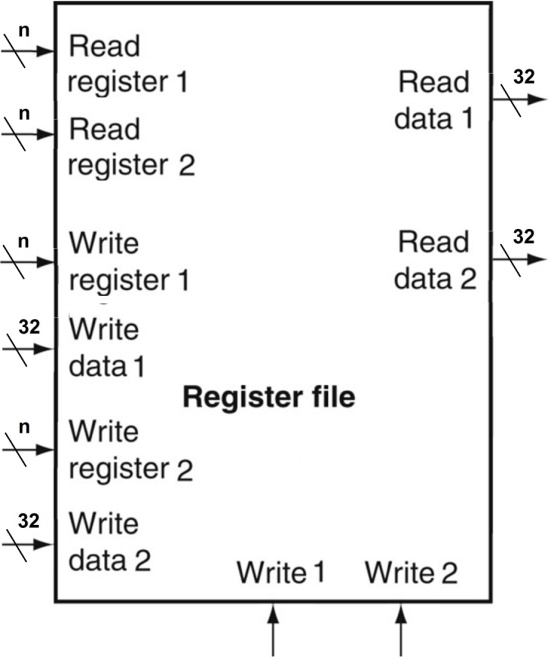
# **Bonus Project: Register File**

**Digital System Modeling using HDL**

**Student Name: Student ID:**

* Include this header with your project.
* In doing this project, you could search the Internet, library, or any other source. ***Please do not copy material from your colleagues***.
* Total: **30 Marks**.
* **Bonus Project:** This is an optional to-submit project.

Using VHDL or Verilog model a register file that contains 2n 32-bit registers. The register file has two read port and two write ports. Below is a symbol of this register file, showing all input and output signals with their bit-widths.



Explain how your model handles the case when both write ports try to write to the same register.

Draw the detailed circuit diagram of your design, showing the bit-width of all input and output signals.

* Propose a test strategy to verify the developed model.
* Develop a testbench to implement the proposed test strategy.
* Run the developed testbench to verify the modeled register file.
* Clearly document your model and testbench code.
* Document the proposed test strategy.
* Include resultant waveforms in your project documentation.

***End of Assignment***